Post-print version:

Optimal control of voltage source converters under power system faults

F.D. Bianchi, A. Egea-Àlvarez, A. Junyent Ferre and O. Gomis-Bellmunt

This work has been published in **Control Engineering Practice**:

F.D. Bianchi, A. Egea-Àlvarez, A. Junyent Ferre and O. Gomis-Bellmunt, "Optimal control of voltage source converters under power system faults", *Control Engineering Practice*, vol. 20, no. 5, pp. 539-546, 2012.

Final version available at:

URL: http://www.sciencedirect.com/science/article/pii/S0967066112000238

DOI: 10.1016/j.conengprac.2012.01.009

BibTex:

```
@Article{Bianchi2012,
    Title    = {Optimal control of voltage source converters under power system
       faults},
    Author   = {Fernando D. Bianchi and Agustí Egea-Àlvarez and Adrià Junyent Ferre
       and Oriol Gomis-Bellmunt},
    Journal  = {Control Engineering Practice},
    Year     = {2012},
    Number   = {5},
    Pages    = {539-546},
    Volume   = {20},
    Doi      = {10.1016/j.conengprac.2012.01.009}
}
```

Optimal control of voltage source converters under power system faults

F.D. Bianchi[a,*], A. Egea-Alvarez[b], A. Junyent-Ferré[b], O. Gomis-Bellmunt[b,a]

[a] *Catalonia Institute for Energy Research, IREC*
Jardins de les Dones de Negre 1, 08930 Sant Adrià de Besòs (Barcelona) Spain
[b] *Centre d'Innovació Tecnològica en Convertidors Estàtics i Accionaments (CITCEA-UPC)*
Universitat Politècnica de Catalunya,
Av. Diagonal 647, Pl. 2, 08028 Barcelona, Spain

Abstract

For the integration of renewable energy in power systems, Voltage Source Converters (VSCs) must transfer power from a DC source to an AC grid with effective control of the DC voltage. An important demand is that the converters remain connected to the grid even under severe voltage perturbations. In these situations, the power transfer capability of the converter suffers a drastic reduction, which may cause over-voltages. In this paper, a multi-variable optimal control with anti-windup compensation is proposed with the aim of improving performance, especially under severe voltage faults. The proposed control scheme is evaluated by simulations using a detailed model of the VSC.

Keywords:
Renewable energy systems, voltage source converters, grid integration, optimal control, windup

1. Introduction

Voltage Source Converters (VSCs) (Yazdani and Iravani, 2010) are used in a number of applications, ranging from low voltage microgrid applications (Sao and Lehn, 2008) to VSC-HVDC[1] large power converters for offshore wind

*Corresponding author. Phone: +34 93 3562615 / Fax: +34 93 3563802.
Email address: fbianchi@irec.cat (F.D. Bianchi)
[1] High Voltage Direct Current

power (Gomis-Bellmunt et al., 2010). Compared to Line Commutated Converters (LCCs) (Arrillaga et al., 2009), VSCs present the advantages of independent control of reactive and active power, black-start capability, no commutation failure, no voltage polarity reversal needed to reverse power, smaller output filters because of the use of high frequency switching and faster dynamics. On the other hand, LCCs can be utilized for higher voltage and power and have fewer losses than VSCs.

Historically, VSC controller designs have been classified into two groups: those based on linear vector control (Perez et al., 2004; Roncero-Sánchez et al., 2009; Magri et al., 2010) and those based on nonlinear control (Malesani and Tomasin, 1993; Kazmierkowski and Malesani, 1998). Linear vector control design methods use an averaged model of the converter, usually combined with the Park transformation, which makes it possible to use regular PI controllers, and have proved to provide a reasonably good performance while being easy to design and analyze due to the availability of linear systems theory tools (Buso, 2006). On the other hand, nonlinear control techniques, the most well known of which is the Direct Power Control (DPC) (Noguchi et al., 1998), take into account the discrete nature of the switching state of the converter and can sometimes obtain a faster response and more robustness to deviations of system parameters, although it is harder to study the behavior of the system. Even though the basic forms of these techniques work well in most common situations, the performance of the system can be improved by using other control techniques. Particularly in the event of severe voltage perturbations, optimal control schemes can improve the system ride-through capability, which is fundamental for the integration into the grid of renewable generation systems. The ride-through capability indicates the ability of the VSC to remain connected during a voltage fault in the grid.

In this paper, a multi-variable optimal control approach is proposed with the aim of improving the ride-through capability of the VSC. The control strategy maintains the classical structure of two loops used in linear approaches, an inner loop controlling the currents and an outer loop regulating the DC volt-

age. This partition is still necessary to limit the currents in the converter. The ride-through capability is enhanced with a third control inspired by anti-windup (AW) compensation concepts. This control is only active during severe voltage sags, where the current demanded by the power transfer exceeds the converter limits. In these cases, the third controller acts on a DC chopper to dissipate the part of the incoming power that cannot be transferred from one side to the other. Although involving a more complex implementation than classical PI structures, this optimal alternative to control VSC provides a more formal and more systematic design procedure and an improvement in the general performance, especially under several voltage sags.

The paper is organized as follows. Section 2 presents the description and modeling of the VSC under analysis. The main contributions can be found in Section 3, where the optimal control strategy is proposed. In Section 4, the new control strategy is evaluated by simulations under several scenarios using a detailed model including the switching of the electronic devices. Finally, in Section 5, some concluding remarks are presented.

2. System description

A two-level VSC exchanging power between a three-phase three-wired grid and a DC source is sketched in Figure 1. The converter consists of three branches with two IGBTs (Isolated Gate Bipolar Transistors) whose middle point is connected to the grid by means of inductors. A Space Vector Modulation (SVM) algorithm controls the IGBTs and generates the desired three-phase voltages on the AC side, thus controlling the active and reactive power flow. The voltages generated in the middle points of the IGBT branches are filtered with inductors for smooth integration into the grid. An additional IGBT and a resistor are used as a DC chopper to mitigate the effects of severe voltage disturbances.

The DC side is connected to a generation or storage source, *e.g.* batteries in photovoltaic systems or the DC side of other converters in wind power systems. In all cases, the VSC transfers the power injected by the DC source into the AC

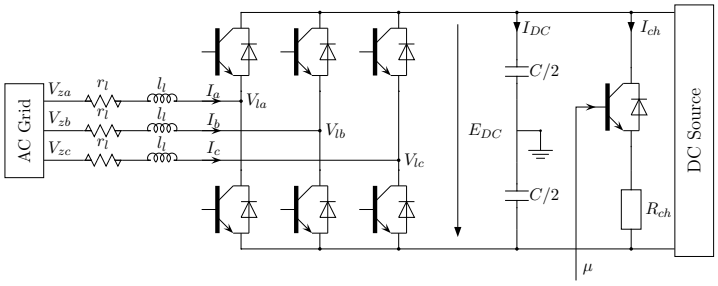

Figure 1: VSC converter with a DC chopper connected to a three-phase three-wired utility grid and a DC source

side. The main objective of the control system is to ensure that the DC voltage remains nearly constant. For this purpose, it is necessary to maintain a balance between the incoming and the outgoing power. However, this balance is only possible if the current limitations are not reached. For example, under severe voltage sags in the AC grid, the currents may reach the limits imposed by the thermal characteristics of the converter. These limitations restrict the amount of power that can be transferred from one side to the other. As a consequence, the excess of power is transferred to the capacitor, producing an increment in the DC voltage that may activate the over-voltage protections. To ride-through the fault, the control must prevent the protections from disconnecting the converter from the grid. When a reduction of the incoming power is not possible, the only option to avoid over-voltages at the DC bus is to dissipate the excess power, which is the purpose of the DC chopper, where the control of the IGBT allows to decide the amount of power dissipated.

For control design purposes, it is common to employ an averaged model where high frequency switching phenomena are neglected. This permits us to model the system in Figure 1 as three AC voltage sources and a DC current source with a capacitive branch (see Figure 2). The current provided by this source is a function of the power flow between the AC and DC sides.

In balanced systems, a three-phase sinusoidal voltage (in the *abc* frame) can be projected into another frame where these variables are fully characterized by

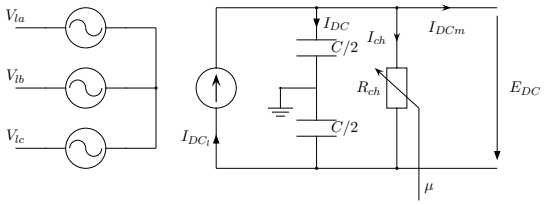

Figure 2: Simplified model of a VSC converter with a DC chopper

two DC magnitudes. This projection is known as a Park transformation and produces two components, the quadrature component q and the direct component d. In the dq frame, the currents in the AC side are described by the following equation:

$$\frac{d}{dt}\begin{bmatrix} i_q \\ i_d \end{bmatrix} = \begin{bmatrix} -r_l/l_l & \omega_e \\ -\omega_e & -r_l/l_l \end{bmatrix}\begin{bmatrix} i_q \\ i_d \end{bmatrix} + \begin{bmatrix} -1/l_l & 0 \\ 0 & -1/l_l \end{bmatrix}\left(\begin{bmatrix} v_{lq} \\ v_{ld} \end{bmatrix} - \begin{bmatrix} v_{zq} \\ v_{zd} \end{bmatrix}\right) \quad (1)$$

where i_d and i_q are the dq currents, v_{ld} and v_{lq} are the converter dq voltages, v_{zd} and v_{zq} are the grid dq voltages, and ω_e is the electrical angular velocity. The latter variable will be assumed constant during the design stage. The grid voltages are projected into a voltage oriented synchronous reference frame, which implies that v_{zd} can be assumed to be zero. With the exception of faults in the grid, the voltage v_{zq} remains constant and is measured in real-time.

The transfer function from the voltage to the currents will be denoted by $G(s)$, *i.e.*,

$$\begin{bmatrix} i_q \\ i_d \end{bmatrix} = G(s)\left(\begin{bmatrix} v_{lq} \\ v_{ld} \end{bmatrix} - \begin{bmatrix} v_{zq} \\ 0 \end{bmatrix}\right).$$

The active and reactive powers in the dq frame are given by

$$P = \frac{3}{2}v_{zq}i_q, \qquad Q = \frac{3}{2}v_{zq}i_d,$$

respectively. Because v_{zq} is usually constant in normal operation, the current i_q is associated with the active power and the current i_d with the reactive power.

The voltage at the DC bus E_{DC} is governed by

$$\frac{dW}{dt} = \frac{2}{C}\left(\frac{3}{2}v_{zq}i_q - P_m - P_{ch}\right) \quad (2)$$

where $W = E_{DC}^2$, $3v_{zq}i_q/2$ is the power injected into the AC side, $P_m = I_{DCm}E_{DC}$ is the power transferred from the DC side and P_{ch} is the power dissipated in the DC chopper.

The DC chopper is modeled as a variable resistor controlled by the signal μ. Thus, the current flowing through this resistor is proportional to μ, *i.e.*,

$$I_{ch} = \frac{E_{DC}}{R_{ch}}\mu.$$

When $\mu = 0$, the current I_{ch} is zero (the IGBT in the chopper branch is turned off), whereas, when $\mu = 1$, the maximum current is passing through the resistor R_{ch}.

3. Control strategy

The proposed control scheme is depicted in Figure 3. The strategy consists of three controllers forming a structure of two nested loops. The controller K_c, in the inner loop, maintains the currents at the desirable values i_q^* and i_d^*, whereas K_v, in the outer loop, regulates the voltage at the DC bus. Both controllers are designed for normal operation, where the currents are below their saturation limits. The control scheme also includes two feedforward terms. The first subtracts the voltage v_{zq} at the q component of the output of the controller K_c. The second subtracts the power incoming from the DC source P_m at the output of the controller K_v.

The outer loop also includes a limitation of the current i_q^* imposed by the voltage controller, which prevents the activation of over-current protections and allows the converter to remain connected during severe faults. The third controller K_{ch} only acts during severe voltage sags, when the current i_q^* exceeds its safety limits and $\bar{i}_q^* \neq i_q^*$. This last controller determines the connection time of the chopper resistor R_{ch} and, as will be seen later, its design is based on AW concepts.

The inputs to the control algorithm are the currents and voltages in the AC side (V_{za}, V_{zb}, V_{zc} and I_a, I_c, respectively) which are converted into the

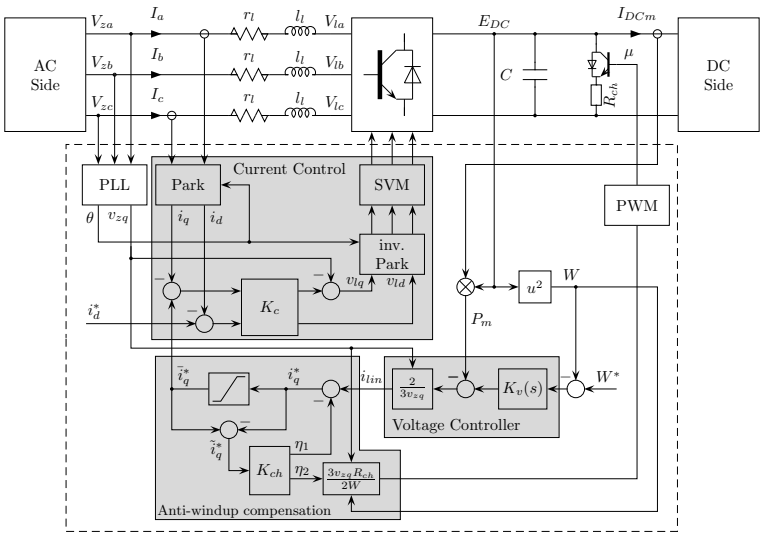

Figure 3: Closed loop system with the proposed control scheme

dq frame by the Park transformation. From the DC side, the inputs are the voltage at the DC bus E_{DC} and the current injected from the DC source I_{DCm}. The control variables are computed first in the dq frame (v_{lq} and v_{ld}) and then converted into the abc frame by the inverse Park transformation. These voltages in the abc frame enter into the SVM algorithm to generate the switch signals commanding the IGBT branches. The Phase-Locked Loop (PLL) determines the component q of the grid voltage (v_{zq}) and the angle θ needed in the direct and inverse Park transformations.

3.1. Normal operation

In normal operation, only the controllers K_c and K_v are active. If the current limit is not reached, $\bar{i}_q^* = i_q^*$ and the input to the controller K_{ch} is zero. The control of the inner and the outer loops is addressed with $\mathcal{H}_\infty$ optimal control techniques (Sánchez Peña and Sznaier, 1998). Although the PI structure is commonly used in VSCs, the $\mathcal{H}_\infty$ tools are capable of considering the interaction among system variables, thus avoiding the need for additional decoupling terms. The resulting controllers may be more effective than decentralized controllers

because the interactions are considered and exploited during the design with the aim of achieving better performance. In addition to provide a more flexible design, $\mathcal{H}_\infty$ optimal control is able to consider model uncertainty (Sánchez Peña and Sznaier, 1998). Although the model uncertainty associated with changes in the system parameters is not considered in the present work, these ideas are used later in the AW compensation used during the fault operation.

The controller K_c has two inputs and two outputs, and its design is cast in the form of a mixed-sensitivity problem. The design objective is to minimize the current errors, $e_{i_q} = i_q^* - i_q$ and $e_{i_d} = i_d^* - i_d$, at low frequencies with reasonable control inputs v_{lq} and v_{ld}. In the context of $\mathcal{H}_\infty$ control, these specifications imply the minimization of the infinity norm of the weighted transfer T_{zw} between the fictitious variables

$$w = [i_q^* \; i_d^*]^T,$$
$$z = [\tilde{e}_{i_q} \; \tilde{e}_{i_d} \; \tilde{v}_{lq} \; \tilde{v}_{ld}]^T,$$

where the "˜" over the symbols denotes the variable after passing through a weighting function. In particular, $\tilde{e}_{i_q}$ and $\tilde{e}_{i_d}$ are the errors weighted with the integral action and the function W_e with the aim of ensuring zero steady-state errors. Similarly, $\tilde{v}_{lq}$ and $\tilde{v}_{ld}$ are weighted with W_u, usually a high pass filter, to avoid large values of the control action. The integral action is placed in the loop during the design and then added to the final controller, *i.e.*, $K_c(s) = (1/s)\bar{K}_c(s)$, where $\bar{K}_c(s)$ is the controller obtained by the optimization algorithm. This factorization is necessary to satisfy stabilizability conditions (see (Zhou et al., 1996) for more details). The control setup passed to the optimization algorithm is shown in Figure 4.

The purpose of the outer loop is to maintain the DC bus voltage E_{DC} by imposing a suitable current reference i_q^* on the inner loop. According to (2), the system to be controlled is governed by

$$\frac{dW}{dt} = \frac{2}{C}\left(\frac{3}{2} v_{zq} i_q\right), \tag{3}$$

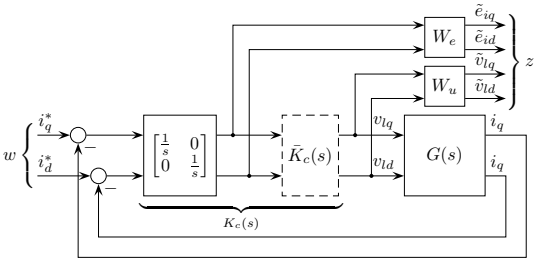

Figure 4: Problem setup for the inner loop passed to the design algorithm

where

$$i_q(s) = T_{i_q^* i_q}(s) i_q^*(s),$$

and $T_{i_q^* i_q}(s)$ is the transfer function from i_q to i_q^* after closing the inner loop with the controller K_c. In normal operation, $P_{ch} = 0$, and P_m is cancelled by the feedforward term. Taking into account that v_{zq} is a measured variable, Equation (3) can be linearized by pre-multiplying it by the factor $2/3v_{zq}$. Thus, the complete voltage controller gives

$$\bar{K}_v = \frac{2}{3v_{zq}} K_v, \tag{4}$$

where K_v can be computed with linear tools such as $\mathcal{H}_\infty$ optimal control. Note that (4) is a gain-scheduled controller, where v_{zq} is the scheduling variable.

The controller K_v has only one input and one output because it only acts on the component q of the reference currents. The current i_d^* is set by the reactive power requirements. After factorization, the problem setup is similar to the case of the inner loop. In this case, the objective is to minimize the difference between $W = E_{DC}^2$ and its reference W^* with a reasonable control input i_q^*. In this case, $w = W^*$ and $z = [\tilde{W}\ \tilde{i}_q^*]^T$, where $\tilde{W}$ is obtained after passing through an integrator and W_e.

3.2. Severe voltage fault operation

During severe voltage faults, the current i_q needed to preserve the entire power transfer may exceed the converter limits. To prevent this situation, the reference current i_q^* is limited, as Figure 3 shows. Under this circumstance, the

control variable in the outer loop is saturated. This fact, along with slow poles or integral action, may cause undesirable overshoots in the controlled variable known as windup. In the case of the VSC, due to the saturation of i_q^*, the controller is not able to reduce the current through the capacitor C to zero and thus causing the windup of the DC voltage.

An option to avoid the saturation of the current i_q^* is to design the controller in such a way that the control input never reaches the saturation limits. Linear optimal control is capable of considering this kind of constraint. However, this option results in very conservative designs, and the saturation is avoided at the expense of a significant sacrifice in the performance in normal operation. In cases where the saturation occurs under extreme situations, the anti-windup compensation techniques are more suitable. These techniques permit us to introduce compensation terms that are active only during the saturation and do not affect the behavior during linear operation.

The proposed AW compensation can be observed in Figure 3 and is based on the scheme proposed in (Weston and Postlethwaite, 2000). The input $\tilde{i}_q^*$ to the AW compensator K_{ch} is the difference between the non-saturated control variable i_q^* and the saturated current $\text{sat}(i_q^*) = \bar{i}_q^*$. The AW compensator

$$K_{ch}(s) = \begin{bmatrix} K_{ch1}(s) \\ K_{ch2}(s) \end{bmatrix},$$

subtracts a signal η_1 at the controller output and produces a signal η_2 to control the power dissipated in the resistor R_{ch}. The scheme differs from the classical AW strategies in the absence of a correction term at the controller input. Instead, the correction is applied to the chopper to control the part of the incoming power dissipated in the resistor R_{ch}, which helps to maintain the voltage at the DC bus during severe voltage sags. A correction term at the input of the controller K_v can also help to reduce the undesirable effect of the windup, but it is not sufficient to prevent an increase of the voltage E_{DC}. Eliminating the voltage error at the input of K_v does not ensure a zero current through the capacitor C, and thus it is not possible to guarantee that the DC voltage will not increase.

The power dissipated in the chopper is given by

$$P_{ch} = \frac{E_{DC}^2}{R_{ch}}\mu = \frac{W}{R_{ch}}\mu. \tag{5}$$

Defining $\mu = (3v_{zq}R_{ch}/2W)\eta_2$ and replacing the previous expressions in (2), the following equation is obtained

$$\frac{dx_w}{dt} = \frac{2}{C}\left(i_q - i_m - \eta_2\right),$$

which is a linear equation in the new variables $x_w = (2/3v_{zq})W$ and $i_m = (2/3v_{zq})P_m$.

With the previous change of variables and to design the controller K_{ch}, Figure 3 can be reduced to Figure 5. After some variable manipulations, the controlled variable (during saturation) is given by

$$x_w(s) = \frac{2}{sC}\left(T_{i_q^* i_q}(s)i_{lin}(s) + (K_{ch2}(s) - T_{i_q^* i_q}(s)(1 + K_{ch,1}(s))\tilde{i}_q^*(s)\right),$$

where i_{lin} is the output of the controller $\bar{K}_v(s)$. There are several options to select $K_{ch1}(s)$ and $K_{ch2}(s)$. In particular, if $K_{ch1}(s) = M(s) - 1$ and $K_{ch2}(s) = N(s)$, with $T_{i_q^* i_q} = N(s)M(s)^{-1}$, we obtain

$$x_w(s) = \frac{2}{sC}G(s)i_{lin}(s).$$

This equation reveals that the AW compensator cancels the effect of the saturation on the output, and the response thus coincides with the response of the system without actuator saturation. This cancellation is possible provided that $\eta_2 \leq 2W_{\max}/3R_{ch}v_{zq}$, which corresponds to the maximum power dissipated in R_{ch} ($\mu = 1$).

The systems $M(s)$ and $N(s)$ are the coprime factors of $T_{i_q^* i_q}(s)$, and they can be computed by solving a state feedback problem (Zhou et al., 1996). If

$$T_{i_q^* i_q}(s) = \left[\begin{array}{c|c} A & B \\ \hline H & D \end{array}\right]$$

then,

$$\begin{bmatrix} M(s) - I \\ N(s) \end{bmatrix} = \left[\begin{array}{c|c} A + BF & B \\ \hline F & 0 \\ H + DF & D \end{array}\right],$$

where F is the state feedback gain to be determined. To guarantee the stability of the AW compensation in Figure 5, the gain F must ensure the stability of the loop formed by the dead zone non-linearity $i_q^* - \text{sat}(i_q^*)$ and $M(s) - I$. In (Weston and Postlethwaite, 2000), it is proved that the condition is satisfied if $\|M(s) - I\|_\infty < 1$, where $\|\cdot\|_\infty$ is the infinity norm. In addition, to prevent η_2 from reaching the maximum implementable value, the optimization problem can include the condition $\|N(s)\|_\infty < \gamma$.

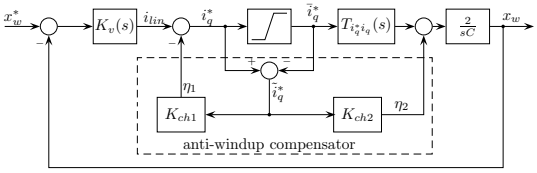

Figure 5: Simplified control scheme for AW compensator design

4. Simulation results

To illustrate the application of the proposed control strategy, an AC grid of 400 V and 50 Hz, a DC bus voltage reference of 800 V and a power converter of 10 kVA of apparent power were considered. The inductor parameters were 0.5 Ω and 5.4 mH. The resistor R_{ch} in the chopper was chosen to be 64 Ω to dissipate 10 kW at 800 V.

The inner and the outer controllers were designed with the Matlab function `hinfmix`, which implements the $\mathcal{H}_2/\mathcal{H}_\infty$ synthesis procedure with pole placement constraints (Scherer et al., 1997). Here, only the $\mathcal{H}_\infty$ constraint was considered but with additional constraints on the closed loop pole locations to implement the controller in discrete time.

The weights for the design of the inner controller were selected to be $W_e = 250 \cdot I_{2\times2}$ and $W_u = 0.01 \cdot I_{2\times2}$, where $I_{2\times2}$ denotes the identity matrix of dimension 2×2. These weighting functions are usually low and high pass filters, respectively, and the setting of their parameters depends on the desired controller bandwidth (Sánchez Peña and Sznaier, 1998). With the previous

values, the design algorithm seeks a controller that ensures small current errors at low frequencies with reasonable voltage control signals. (Remember that W_e weighs the integral of the current errors; see Figure 4.) The closed-loop poles were confined to the sector $\mathbb{S} := \{s \in \mathbb{C} : (|s| \leq 3000) \cap (3\pi/4 \leq \angle s \leq 5\pi/4)\}$, where $\mathbb{C}$ denotes the complex plane. For the computation of the outer controller, the order of the transfer $T_{i_q^* i_q}$ was reduced to avoid a high order controller. The order of the controller produced by the $\mathcal{H}_\infty$ procedures is equal to the order of the plant plus the sum of the orders of any weighting function used to state the specifications. The weights in the outer loop case were also constant ($W_e = 6$ and $W_u = 0.05$). Finally, the AW compensator K_{ch} was designed as mentioned in the previous section by solving a state feedback problem subject to $\|M(s) - 1\|_\infty < 1$ and $\|N(s)\|_\infty < \gamma$.

The controller design is based on the average model, as described in the previous section. Therefore, to verify this approximation, the controllers were evaluated with a more detailed model implemented in SimPowerSystems for Matlab/Simulink. The model includes seven switching devices, six to implement the inverter and one for the chopper. The switching signals commanding the inverter IGBTs are generated with the SVM algorithm shown in Figure 6. The algorithm takes as inputs the DC voltage E_{DC} and the $\alpha\beta$ components of the dq voltages produced by the current controller. The $\alpha\beta$ components can be obtained from v_{lq} and v_{ld} after applying the Clarke transformation. The outputs of the SVM algorithm are the switching signals q^{abc} and $\bar{q}^{abc}$; see (Bose, 2001) for more details. The switching signal for the chopper is computed by a simple PWM algorithm comparing the value of μ and the triangular signal of 20 kHz. The three linear controllers are discretized by means of the Tustin transformation for a sample frequency of 20 kHz coincident with switching frequency of the SVM algorithm. These controllers are given in the Appendix.

With the aim of comparison, a classical PI control scheme was also evaluated along with an on-off strategy to control the DC chopper. In the inner loop, the PI controller was tuned according to $K_p = l_l/\tau$ and $K_i = r_l/\tau$, where K_p and K_i are the proportional and integral constants, respectively, and τ is the desired

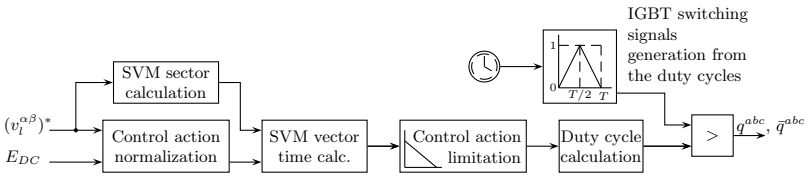

Figure 6: SVM algorithm for the switching signal generation

time constant of the current loop (in this case, $\tau = 1$ ms). The gains of the voltage loop controller are $K_p = \tau C/\sqrt{2}$ and $K_i = \tau^2 C/2$ (Buso, 2006). The on-off control of the DC chopper is basically a sign function with a hysteresis block fed with the DC voltage error (Arulampalam et al., 2006). A classical anti-windup compensation (a constant gain) was also added to the voltage loop to prevent large voltage deviations after the voltage faults.

Two scenarios were evaluated: a change in the active power injected from the DC power source and a voltage sag in the AC electrical grid. In the first scenario, the control remains in normal operation, whereas, in the second, the AW compensator and the DC chopper are needed to maintain the voltage at the DC bus almost constant.

Figures 7 to 9 present the simulation results for the first scenario. The active power injected from the DC side increases from 4.5 kW to 9 kW during a 100 ms period starting at 0.05 s. Figure 7a shows the dq currents with the corresponding references (dashed lines), where i_q^* is the reference produced by the outer controller to maintain the E_{DC} at 800 V. The abc currents are shown in Figure 7b. In Figures 7c and d, the active power and the voltage at the DC bus are shown with the results obtained with the PI control strategy. Comparing both controllers shows some improvement in the optimal scheme. The power and the DC voltage present a slightly faster convergence to the nominal values although with a slightly higher deviation of the DC voltage during the changes in the power. It can be also noted that, except for a very short period of time, the currents do not exceed their limits, which are indicated with dotted lines (± 20.41 A). The voltages in the dq are shown in Figure 8a and the voltages in

the *abc* frame in Figure 8b. A detail of the *abc* currents and the control voltages produced by the inverter are shown in Figure 9.

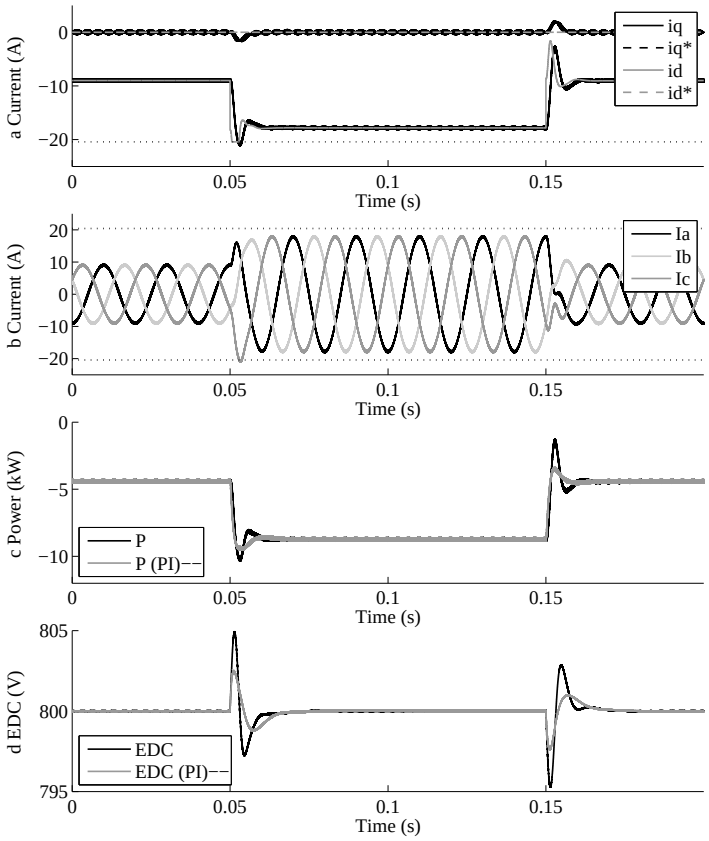

Figure 7: Simulation corresponding to the power change scenario. a) Currents in the *dq* frame, b) currents in the *abc* frame, c) active power and d) voltage at the DC bus

The second scenario corresponds to a 80% voltage sag with a duration of 500 ms, in accordance with the ride-through requirements imposed by the Spanish grid code for wind farm integration (P.O. 12.3, 2006). The responses of the system are shown in Figures 10 to 12. The first figure presents the *dq* and the *abc* voltages in the grid and in the converter. In this scenario, the controller input does not exceed the maximum voltage levels (461.88 V), and thus no saturation effects are observed in the inner loop. The currents and the corresponding

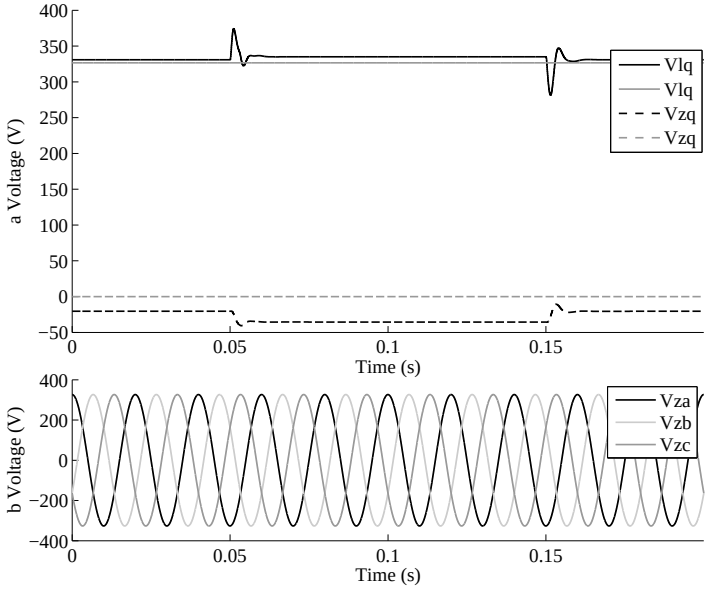

Figure 8: Simulation corresponding to the power change scenario. a) Voltages in the *dq* frame and b) grid voltages in the *abc* frame

references in the *dq* and *abc* frames are shown in Figure 11a. Observe that the maximum current limits (dotted lines) are reached during the voltage sag, and, as a consequence, the DC chopper is active during the fault. Figure 12 presents the DC voltage and the current in the chopper. Notice that the AW mechanism is only active to compensate the fault.

Figures 11 and 12 also include (grey lines) results obtained when the classical control scheme (PI plus AW and on-off control of the chopper) is used instead of the proposed optimal control alternative. These simulations reveal that the proposed strategy achieves a better voltage regulation even in an extreme scenario such as a 80% voltage sag, compared with the results of the case of classical control. The classical approach exhibits a slow convergence to the nominal voltage after a disturbance. Larger voltage deviations are observed in the classical scheme case as a consequence of the fact that the PI controller continues integrating because the on-off control of the chopper is not capable of

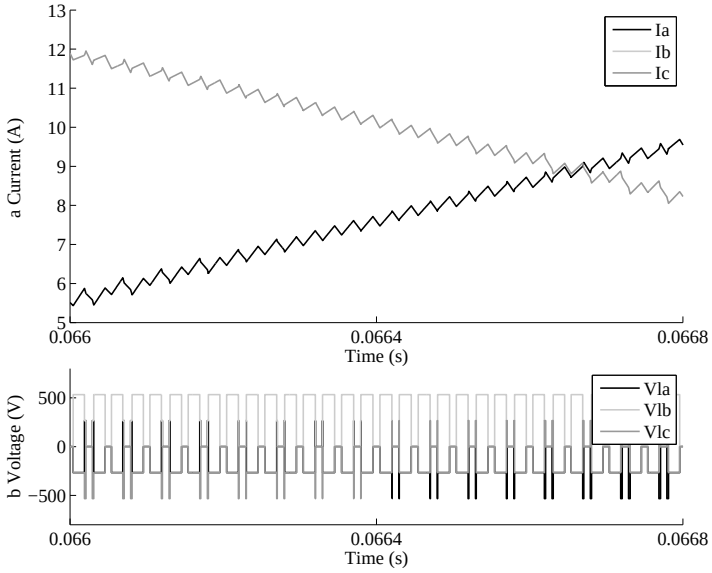

Figure 9: Simulation corresponding to the power change scenario. a) Detail of the *abc* currents and b) control voltages in the *abc* frame

forcing the voltage error toward zero. Unlike the optimal option, the implementation of the on-off control of the chopper requires an offset in the DC voltage. The voltage deviation in the classical scheme could be reduced by increasing the AW gain, but this strategy can also affect the stability. This effect is not observed in the proposed AW scheme, which not only permits a more flexible and systematic design but also ensures the closed loop stability.

5. Conclusions

A scheme of three optimal controllers has been proposed for the control of VSC with DC choppers during normal operation and under severe voltage faults. In normal operation, two control loops regulate the voltage at the DC bus during the power transfer between the DC and the AC side. Under severe voltage faults, where the power transfer capability of the system suffers a drastic reduction, an AW compensator controls the power dissipated in the DC chopper to maintain the voltage, allowing the converter to remain connected to the grid.

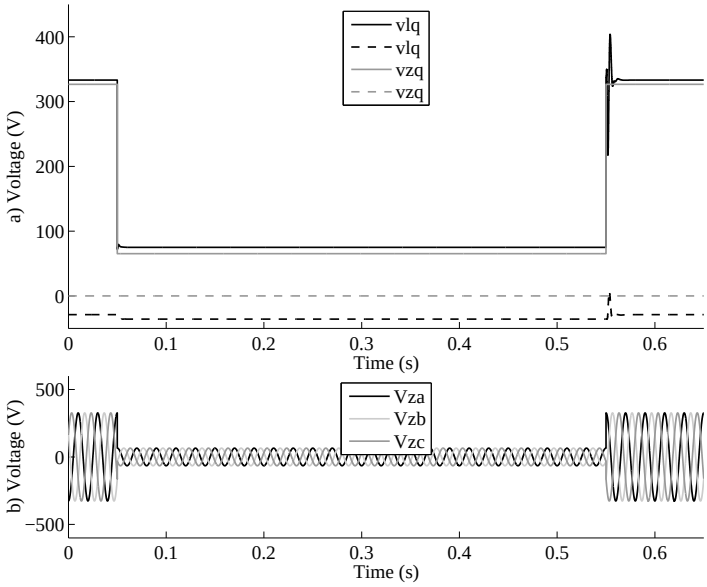

Figure 10: Simulation corresponding to the voltage sag scenario. a) Voltages in the *dq* frame and b) grid voltages in the *abc* frame

The new scheme was evaluated by simulations and compared with classical controls based on non-interactive PI structures. The simulations reveal certain performance improvements in normal operation. Nevertheless, the most noticeable improvement was observed under severe voltage sags where the chopper is needed to maintain the DC voltage close to its rated value. In this situation, the optimal AW controller provides a more effective control of the chopper, achieving a faster convergence of the DC voltage and ensuring stability in only one AW compensation design step.

From the implementation viewpoint, the proposed control scheme is somewhat more complex, and the order of the controllers is higher than in classical PI. Nevertheless, these controllers are linear time-invariant systems, and they are implemented as difference equations similar to PI controllers. On the other hand, the additional complexity of the implementation is compensated by the improvement in the ride-through capability of the VSC.

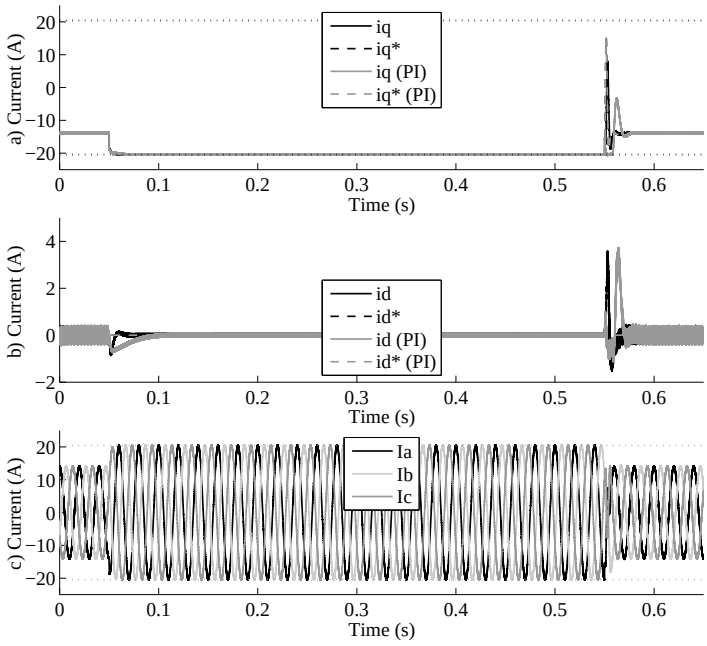

Figure 11: Simulation corresponding to the voltage sag scenario; the black lines correspond to the proposed scheme and the grey lines to the classical PI control scheme. a) Component q of the current, b) component d of the currents and c) currents in the abc frame

Acknowledgement

This work was supported by the *Ministerio de Ciencia e Innovación (Spain)* under the projects ENE2009-08555, DPI2008-00403 and by EIT KIC-Innoenergy under the project OFFWINDTECH.

References

J. Arrillaga, Y. Liu, N. Watson, and N. Murray. *Self-Commutating Converters for High Power Applications.* Wiley, 2009.

A. Arulampalam, M. Barnes, N. Jenkins, and J.B. Ekanayake. Power quality and stability improvement of a wind farm using STATCOM supported with

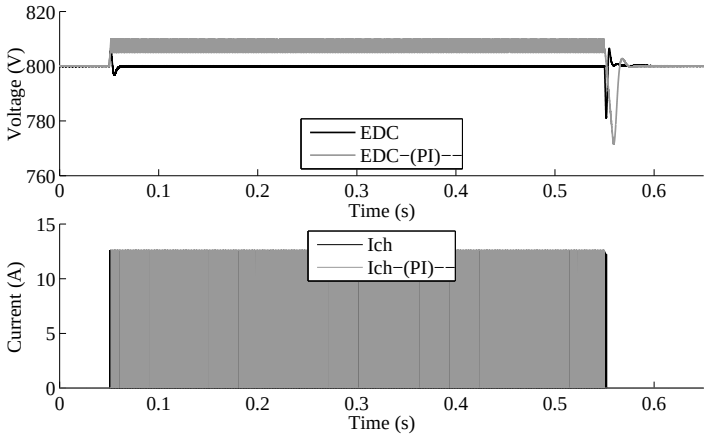

Figure 12: Simulation corresponding to the voltage sag scenario, comparison between the proposed control (black lines) and classical PI control strategy (grey lines). a) DC voltages and b) currents in the chopper

hybrid battery energy storage. *IEE Proceedings-Generation, Transmission and Distribution*, 153(6):701–710, 2006.

B. K. Bose. *Modern Power Electronics and AC Drives*. Prentice Hall, 2001.

S. Buso. *Digital Control in Power Electronics (Synthesis Lectures on Power Electronics)*. Morgan and Claypool Publishers, 2006. ISBN 1598291122.

O. Gomis-Bellmunt, J. Liang, J. Ekanayake, and N. Jenkins. Topologies of multiterminal HVDC-VSC transmission for large offshore wind farms. *Electric Power Systems Research*, 2010.

M.P. Kazmierkowski and L. Malesani. Current control techniques for three-phase voltage-source PWM converters: a survey. *IEEE Transactions on Industrial Electronics*, 45(5):691–703, 1998. doi: 10.1109/41.720325.

A. El Magri, F. Giri, A. Abouloifa, and F.Z. Chaoui. Robust control of synchronous motor through AC/DC/AC converters. *Control Engineering Practice*, 18(5):540 – 553, 2010. doi: DOI: 10.1016/j.conengprac.2010.02.005.

L. Malesani and P. Tomasin. PWM current control techniques of voltage source converters-a survey. In *Proceedings of the International Conference on Industrial Electronics, Control, and Instrumentation (IECON)*, pages 670–675, 1993. doi: 10.1109/IECON.1993.339000.

T. Noguchi, H. Tomiki, S. Kondo, and I. Takahashi. Direct power control of PWM converter without power-source voltage sensors. *IEEE Transactions on Industry Applications*, 34(3):473–479, 1998. doi: 10.1109/28.673716.

M. Perez, R. Ortega, and J.R. Espinoza. Passivity-based PI control of switched power converters. *IEEE Transactions on Control Systems Technology*, 12(6): 881–890, 2004. doi: 10.1109/TCST.2004.833628.

P.O. 12.3. *Requisitos de respuesta frente a huecos de tensión de las instalaciones eólicas*. Ministerio de Industria, Turismo y Comercio, Spain, 2006.

P. Roncero-Sánchez, V. Feliu-Batlle, and A. García-Cerrada. Design and comparison of state-feedback and predictive-integral current controllers for active- and reactive-power control in renewable energy systems. *Control Engineering Practice*, 17(2):255 – 266, 2009. doi: 10.1016/j.conengprac.2008.07.003.

C.K. Sao and P.W. Lehn. Control and power management of converter fed microgrids. *IEEE Transactions on Power Systems*, 23(3):1088–1098, 2008.

C. Scherer, P. Gahinet, and M. Chilali. Multiobjective output-feedback control via LMI optimization. *IEEE Transactions on Automatic Control*, 42(7):896–911, 1997. doi: 10.1109/9.599969.

R.S. Sánchez Peña and M. Sznaier. *Robust Systems Theory and Applications*. John Wiley & Sons, Inc., 1998.

P. Weston and I. Postlethwaite. Linear conditioning for systems containing saturating actuators. *Automatica*, 36(9):1347–1354, 2000. doi: 10.1016/S0005-1098(00)00044-3.

A. Yazdani and R. Iravani. *Voltage-Sourced Converters in Power Systems*. Wiley, 2010.

K. Zhou, John C. Doyle, and Keith Glover. *Robust and Optimal Control*. Prentice-Hall, 1996.

Appendix

Controllers used in simulations

$$K_c(z) = \left[\begin{array}{cccccc|cc} 1.000 & 0.000 & 0.000 & 0.000 & 0.000 & 0.000 & -2.212 & 0.000 \\ 0.000 & 1.000 & 0.000 & 0.000 & 0.000 & 0.000 & -0.000 & -2.212 \\ 0.000 & 0.000 & 0.943 & 0.011 & -0.122 & 0.001 & -0.426 & -0.304 \\ 0.000 & 0.000 & -0.011 & 0.943 & -0.001 & -0.122 & 0.304 & -0.426 \\ 0.000 & 0.000 & 0.121 & 0.014 & 0.785 & -0.014 & 0.327 & 0.303 \\ 0.000 & 0.000 & -0.014 & 0.121 & 0.014 & 0.785 & -0.303 & 0.327 \\ \hline 0.018 & 0.019 & 0.340 & -0.398 & 0.293 & -0.336 & -0.030 & 0.001 \\ -0.019 & 0.018 & 0.398 & 0.340 & 0.336 & 0.293 & -0.001 & -0.030 \end{array}\right]$$

$$K_v(z) = \left[\begin{array}{ccccc|c} 1.000 & 0.000 & 0.000 & 0.000 & 0.000 & -0.624 \\ 0.000 & 0.932 & 0.138 & 0.083 & -0.003 & 0.229 \\ 0.000 & -0.138 & 0.969 & -0.061 & 0.005 & 0.090 \\ 0.000 & -0.083 & -0.061 & 0.698 & 0.122 & 0.147 \\ 0.000 & -0.003 & -0.005 & -0.122 & 0.982 & 0.009 \\ \hline -0.005 & 0.229 & -0.090 & -0.147 & 0.009 & 0.008 \end{array}\right]$$

$$K_{ch}(z) = \left[\begin{array}{ccc|c} 0.928 & 0.005 & -0.003 & 0.239 \\ -0.115 & 0.901 & 0.001 & 0.180 \\ -0.003 & -0.006 & 1.000 & 0.005 \\ \hline -0.217 & -0.141 & -0.004 & -0.041 \\ 0.087 & -0.134 & 0.004 & -0.003 \end{array}\right],$$

where the sample frequency is 20 kHz.

List of Figures