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Optimal control of voltage source converters for fault operation

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Keywords

<<Renewable energy systems>>, <<Voltage Source Converter (VSC)>>, <<Fault ride-through>>, <<Optimal control>>, <<Smart microgrids>>.

Abstract

An optimal control scheme for voltage source converters (VSC) is presented. The proposed control is based on multi-variable and anti-windup control ideas with the objective of improving the ride-through capability of the VSC. The proposed scheme is evaluated by simulations and compared with classical controls.

1 Introduction

Voltage source converters (VSC) [1] are used in a number of applications, ranging from low voltage microgrid applications [2] to VSC-HVDC large power converters for offshore wind power [3, 4]. Compared to line commutated converters (LCCs) [5], VSCs present the advantages of independent control of reactive and active power, black-start capability, no commutation failure and no voltage polarity reversal needed to reverse power. On the other hand, LCCs can be utilised for higher voltage and power and has fewer losses than VSC.

The control of VSCs is traditionally addressed designing a voltage PI controller for the DC bus voltage and decoupling and controlling separately the q and d currents in the synchronous reference frame using PI controllers [6]. Although this classical control scheme shows reasonably good performance for normal and fault operation, the dynamic response and robustness of the system can be improved by using other control techniques. Specially in the event of severe voltage perturbations, optimal control schemes can improve the system ride-through capability which is fundamental when dealing with renewable generation integration in the grid.

In this paper, a multi-variable optimal control approach is proposed with the aim of improving the ride-through capability of the VSC. The control strategy maintains the classical partition of two loops, an inner

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one controlling the currents and an outer one maintaining the DC voltage. This partition is still necessary to keep under safety limits the currents in the converter. The ride-through capability is enhanced with a third control inspired in anti-windup compensation. This control acts on a DC chopper in order to dissipate the part the incoming power that can not be transfer from one side to the other during severe voltage sags. Although with more complex implementation than classical PI structures, this optimal alternative to control VSCs provides a more formal and more systematic design procedure. In addition to improve the general performance especially under several voltage disturbances.

2 System description

The system under study, sketched in Figure 1, is a two level Voltage Source Converter (VSC) exchanging power between an AC and a DC grids. The converter consists of three branches with two IGBT whose middle point is connected to the grid by means of inductances. The system also includes a DC chopper with the aim of helping to mitigate the effects of the severe voltage disturbances.

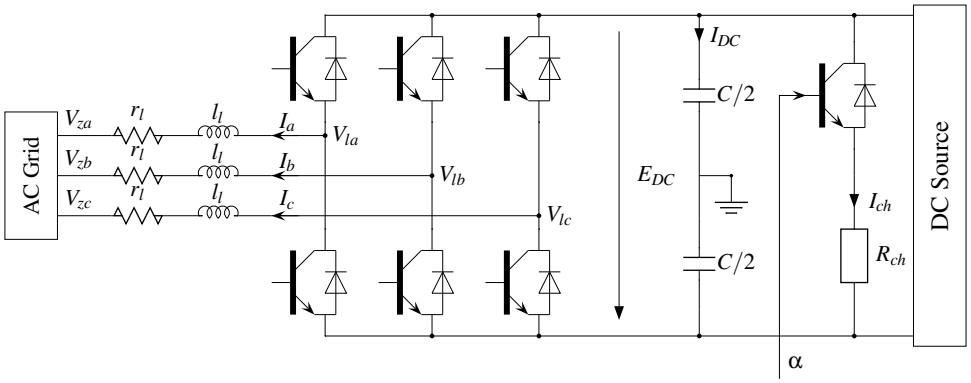

Figure 1: VSC converter connected to a three-phase utility grid and a DC chopper

For the purpose of control design, the system can be modelled as three AC voltage sources and a DC current source with a capacitor branch (see Figure 2). The current provided by this source is a function of the power flow between the AC and the DC sides. The DC chopper is modelled as variable resistor controlled by the signal $\alpha \in [0,1]$. Thus, the current flowing through this resistor is proportional to α, *i.e.*,

$$I_{ch} = \frac{E_{DC}}{R_{ch}}\alpha.$$

When $\alpha = 0$, the current I_{ch} is zero (the IGBT in the chopper branch is turned off); whereas when $\alpha = 1$, the maximum current is passing through the resistor R_{ch}.

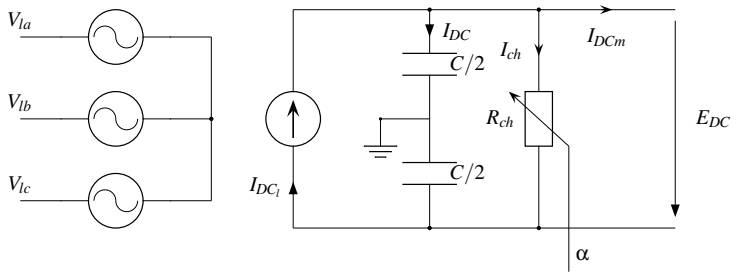

Figure 2: Simplified model of the VSC converter and the DC chopper

In the voltage oriented synchronous reference frame and assuming a balanced grid, the currents in the AC side are described by the following equation

$$\frac{d}{dt}\begin{bmatrix} i_q \\ i_d \end{bmatrix} = \begin{bmatrix} -r_l/l_l & \omega_e \\ -\omega_e & -r_l/l_l \end{bmatrix}\begin{bmatrix} i_q \\ i_d \end{bmatrix} + \begin{bmatrix} -1/l_l & 0 \\ 0 & -1/l_l \end{bmatrix}\left(\begin{bmatrix} v_{lq} \\ v_{ld} \end{bmatrix} - \begin{bmatrix} v_{zq} \\ 0 \end{bmatrix}\right) \tag{1}$$

where i_q and i_d are the qd currents, v_{lq} and v_{ld} are the converter qd voltages, v_{zq} is the grid voltage and ω_e is the electrical angular velocity. This last variable will be assumed constant during the design stage. The transfer function from the voltage to the currents will be denoted by $G(s)$, *i.e.*,

$$\begin{bmatrix} i_q(s) \\ i_d(s) \end{bmatrix} = G(s) \left(\begin{bmatrix} v_{lq}(s) \\ v_{ld}(s) \end{bmatrix} - \begin{bmatrix} v_{zq}(s) \\ 0 \end{bmatrix} \right).$$

The voltage in the DC bus E_{DC} is governed by

$$\frac{dW}{dt} = \frac{2}{C} \left(\frac{3}{2} v_{zq} i_q - P_m - P_{ch} \right) \tag{2}$$

where $W = E_{DC}^2$, $P_m = I_{DCm} E_{DC}$ is the power transferred from the DC side and P_{ch} is the power dissipated in the DC chopper ($P_{ch} = E_{DC}^2 \alpha / R_{ch}$).

3 Control strategy

The proposed control scheme is depicted in Figure 3. The strategy consists of three controllers in a cascade configuration. The controller K_c, in the inner loop, maintains the currents at the desirable values i_q^* and i_d^*, whereas K_v, in the outer loop, regulates the voltage at the DC bus. Both controllers are designed for normal operation where all variables are within safety limits. The third controller K_{ch} only acts during severe voltage faults, when the current i_q^* exceeds its safety limits. This last controller determines the connection time of the chopper resistor R_{ch} and, as will be seen next, its design is based on anti-windup (AW) concepts.

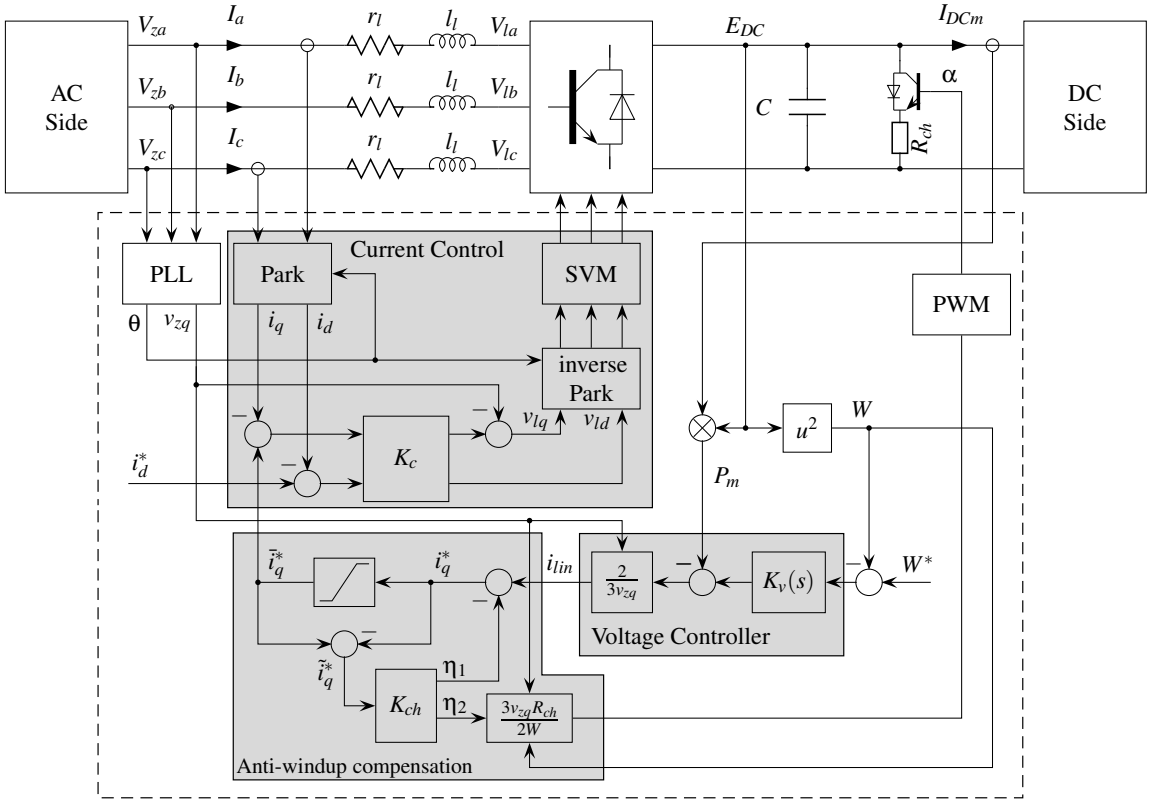

Figure 3: Proposed control scheme

The control algorithm imposes the voltages V_{la}, V_{lb}, V_{lc} by means of space vector modulation (SVM). The control variables are computed first in the qd frame (v_{lq} and v_{ld}) and then converted into the abc frame by the inverse Park transformation. These voltages in the abc frame enter in the SVM algorithm to

produce the switch signals commanding the IGBT branches. The inputs to the control algorithm are the currents and voltages in the AC side (V_{za}, V_{zb}, V_{zc} and I_a, I_c, respectively) which are converted into the *qd* frame by the Park transformation, the voltage in the DC bus and the current injected by the DC source.

3.1 Normal operation

In normal operation, the controller K_c, in the inner loop, acts on the converter voltages v_{lq} and v_{ld} in order to maintain the currents at the desired values given by the references i_q^* and i_d^*. This multi-variable controller is designed using $\mathcal{H}_2$ optimal control techniques [7] (This is basically the standard LQG optimal control but the specifications are introduced in a different form.) The $\mathcal{H}_2$ tools are capable to consider the interaction among system variables and thus avoiding the need of additional decoupling terms. The resulting controllers may be more effective than decentralised controllers since the interactions are considered and exploited during the design with the aim of achieving a better performance.
In $\mathcal{H}_2$ optimal control, the design requires expressing the control problem in terms of the minimisation of the 2-norm of a transfer $T_{zw}(s)$ from an input w to an output z, *i.e.*,

$$\min \|T_{zw}\|_2 = \min_{w \in \mathcal{W}} \|T_{zw} w\|_2 = \min_{w \in \mathcal{W}} \|z\|_2,$$

where $\|z\|_2 = \sqrt{\int z^T z dt}$. The signals w and z are fictitious variables chosen to represent the specifications in the controller design. There are two interpretations of this control formulation. One consists in the minimisation of the energy of the signal z when the system is excited with certain type of input w defined in the set $\mathcal{W}$ (*e.g.*, the set of step functions). An alternative interpretation is to consider the controller design as the minimisation of the extreme values of z when the system is excited with energy bounded signals w (*i.e.*, $\mathcal{W} = \{w : \|w\|_2 < 1\}$). Commonly, the elements in z are weighted by functions of the frequency in order to put more or less emphasis in the minimisation of each element and thus reflecting the relative importance of the different specifications. These weighting functions are basically transfer functions selected in accordance with the frequency content of the desirable objective variables [7].
In the particular case of the inner loop in Figure 3, the specifications consist in minimising the current errors, $e_{i_q} = i_q^* - i_q$ and $e_{i_d} = i_d^* - i_d$, in low frequencies with reasonable control inputs v_{lq} and v_{ld}. In the $\mathcal{H}_2$ format, these specifications imply that $w = [i_q^* \; i_d^*]^T$ and $z = [\tilde{e}_{i_q} \; \tilde{e}_{i_d} \; \tilde{v}_{lq} \; \tilde{v}_{ld}]^T$, where the "~" over the variable denotes the weighted version of the variable. Thus, $\tilde{e}_{i_q}$ and $\tilde{e}_{i_d}$ are the errors after passing through integral action and the weight $W_e(s)$ with the aim of ensuring zero steady-state errors. This emphases the error values in low frequencies and indicates to the optimisation algorithm that the controller must minimise the error in this frequency range. In similar way, the function $W_u(s)$ weights the control variable in order to maintain it bounded and thus avoiding unreasonable values. The problem setup passed to the design algorithm is sketched in Figure 4, where the objective variables are weighted with the functions W_e and W_u. The integral action is placed in the loop during the design and then added to the final controller, *i.e.*, $K_c(s) = 1/s\bar{K}_c(s)$, where $\bar{K}_c(s)$ is the controller produced by the optimisation algorithm. This factorisation is needed to satisfy stabilisability conditions (see [8] for more details). In addition to the feedback controller $K_c(s)$, a feed-forward term v_{zq} is added at the q component of the controller output to improve the current regulation.
The purpose of the outer loop is to maintain the DC bus voltage E_{DC} by imposing a suitable current reference i_q^* to the inner loop. The voltage in the DC bus depends on the power balance between the DC generation source and the power injected into the grid. For instance, a drop in the grid voltage reduces the power transferred to the grid. As consequence, part of the input current is diverted to the capacitor increasing the value of E_{DC}. In order to prevent this situation, the controller $K_v(s)$ in the outer loop increases the current set-point i_q^* balancing the power flow and maintaining the voltage at the DC bus.
In the case of the outer loop, the system to be controlled is given by (2), where

$$i_q(s) = T_{i_q^* i_q}(s) i_q^*(s), \tag{3}$$

and $T_{i_q^* i_q}(s)$ is the transfer function from i_q^* to i_q after closing the inner loop with the controller K_c (in normal operation $P_{ch} = 0$). The controller $K_v(s)$ has only one input and one output since it only acts on

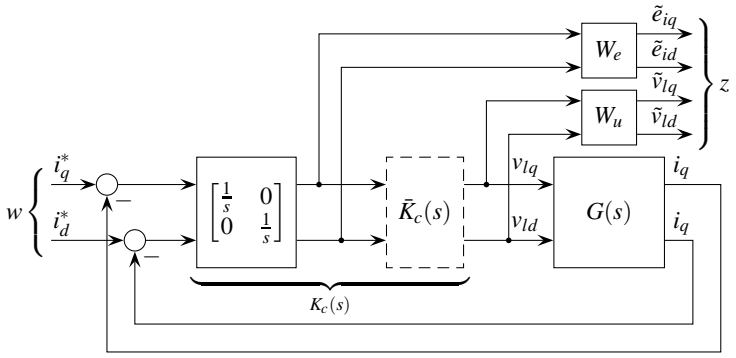

Figure 4: Problem setup for inner loop passed to the design algorithm

the component q of the reference current. The current i_d^* is set by the reactive power requirements. It can be deduced from (2) and (3) that the W is governed by a nonlinear equation due to the product of i_q and v_{zq}. This nonlinear behaviour can be circumvented by factorising the controller as follows

$$\bar{K}_v = \frac{2}{3v_{zq}} K_v. \tag{4}$$

The controller K_v is computed with linear tools and then affected by the gain $2/3v_{zq}$. This can be seen as a gain scheduled controller where v_{zq} is the scheduling variable. Therefore, the controller in the outer loop is also designed employing $\mathcal{H}_2$ tools with a similar objective, *i.e.* to minimise the difference between the $W = E_{DC}^2$ and its reference W^* with a reasonable control input i_q^*. After adding this gain, the controller can be computed using a scheme similar to the one used in the computation of K_c. In this case, $w = W^*$ and $z = [\tilde{W}\ \tilde{i}_q^*]^T$, where $\tilde{W}$ is obtained after passing through an integrator and W_e. A feed-forward term P_m is also included to cancel the change in the incoming power from the DC generation source.

3.2 Severe voltage fault operation

During severe voltage faults, the current i_q may exceed the safety limits. In order to prevent this situations, the reference current i_q^* is limited as Figure 3 shows. Under this circumstance, the control variable in the outer loop is saturated. This fact along with slow poles or integral action may cause undesirable oversteps in the controlled variable, usually referred as control windup. In the case of the VSC, the saturation of i_q^* prevent the controller from ensuring a zero current in the capacitor C and thus causing the windup of the DC bus voltage.

An option to avoid the saturation of the current i_q^* consists in designing the controller such that the control input never reaches the saturation limits. Optimal control is capable of dealing with this kind of constraints. However, in case of linear controllers, this option results in very conservative designs that avoids the saturation at expenses of a significant sacrifice of the performance in normal operation. A more recommended alternatives are the anti-windup compensation techniques which only are active during the saturation and do not affect the behaviour in linear operation.

The proposed anti-windup compensation can be observed in Figure 3 and is based on the scheme proposed in [9]. The input $\tilde{i}_q^*$ to the anti-windup compensator K_{ch} is the difference between the non-saturated control variable i_q^* and the saturated current $\text{sat}(i_q^*) = \bar{i}_q^*$. The anti-windup compensator

$$K_{ch} = \begin{bmatrix} K_{ch1} \\ K_{ch2} \end{bmatrix},$$

subtracts a signal η_1 at the controller output and produces a signal η_2 to control the power dissipated by the chopper resistor R_{ch}. The scheme differs from the classic anti-windup strategies in the fact that there is no correction at the controller input. Instead, the correction is applied at the input of $2/sC$, which models the dissipation of part of the incoming power in the resistor R_{ch}. This allows us to maintain the voltage in the DC bus. A correction at the input of the controller K_v can also help to reduce the

undesirable effect of the windup, but it is not sufficient to prevent an increment of the voltage E_{DC}. Even when the K_v stopped the integration of the error, the current coming from the DC side would continue flowing through the capacitor C and thus the voltage in the DC bus would continue increasing.
The purpose of the DC chopper is to dissipate part of the incoming power from the DC side when the current i_q^* reaches the saturation limits. The power dissipated in the chopper is given by

$$P_{ch} = \frac{E_{DC}^2}{R_{ch}}\alpha = \frac{W}{R_{ch}}\alpha. \tag{5}$$

Therefore, to be able to employ linear tools in the design the anti-windup compensator, the duty cycle α is affected by $3v_{zq}R_{ch}/2W$. Again, the resulting compensator can be seen as a gain-scheduled controller where in this case the scheduling variables are v_{zq} and W. Replacing the previous expressions in (2), we obtain the following equation

$$\frac{d}{dt}x_w = \frac{2}{C}\left(i_q - i_m + \eta_2\right),$$

which is a linear equation in the new variables $dx_w/dt = (2/3v_{zq})dW/dt$ and $i_m = (2/3v_{zq})P_m$.
With the previous change of variables and for the design of the controller K_{ch}, Figure 3 can be reduced to Figure 5. After some variable manipulation, the controlled variable (during saturation) is given by

$$x_w(s) = \frac{2}{sC}\left(T_{i_q^* i_q}(s)i_{lin}(s) + (K_{ch2}(s) - T_{i_q^* i_q}(s)(1+K_{ch,1}(s))\tilde{i}_q^*(s)\right)$$

where i_{lin} is the output of the controller $K_v(s)$. There are several options to select $K_{ch1}(s)$ and $K_{ch2}(s)$. In particular, if $K_{ch1}(s) = M(s) - 1$ and $K_{ch2}(s) = N(s)$, with $T_{i_q^* i_q} = N(s)M(s)^{-1}$,

$$x_w(s) = \frac{2}{sC}T_{i_q^* i_q}(s)i_{lin}(s).$$

This implies that the anti-windup compensator cancels the effect of the saturation on the output and the response will coincide with the response of the system without actuator saturation. This cancellation is possible as long as $\eta_2 \leq 2W_{\max}/3R_{ch}v_{zq}$, which corresponds to the maximum power dissipated in R_{ch} ($\alpha = 1$).
The system $M(s)$ and $N(s)$ are the coprime factors of $T_{i_q^* i_q}(s)$ and they can be computed by solving a state feedback problem. If

$$T_{i_q^* i_q}(s) = C(sI - A)^{-1}B + D$$

then,

$$\begin{bmatrix} M(s) - 1 \\ N(s) \end{bmatrix} = \begin{bmatrix} F \\ C + DF \end{bmatrix}(sI - A - BF)^{-1}B + \begin{bmatrix} 0 \\ D \end{bmatrix},$$

where F is the state feedback gain to be determined. In order to guarantee the stability of the anti-windup compensation in Figure 5, the gain F must ensure the stability of the loop formed by the non-linearity $i_q^* - \text{sat}(i_q^*)$ and $(M(s) - 1)$. In [9], it is proved that the condition is satisfied if $\|M(s) - I\|_\infty < 1$, where $\|\cdot\|_\infty$ is the infinity norm. In addition, to prevent η_2 from reaching the maximum implementable value, the optimisation problem can include the condition $\|N(s)\|_\infty < \gamma$. This optimisation problem can be solved with standard Matlab functions.

4 Simulation results

In order to illustrate the application of the proposed control strategy, it is considered an AC grid of 400 V and 50 Hz, a DC bus voltage reference of 800 V and a power converter of 10 kVA of apparent power. The inductor parameters are 0.5 Ω and 5.4 mH. The resistor R_{ch} in the chopper was chosen of 64 Ω to dissipate 10 kW at 800 V.

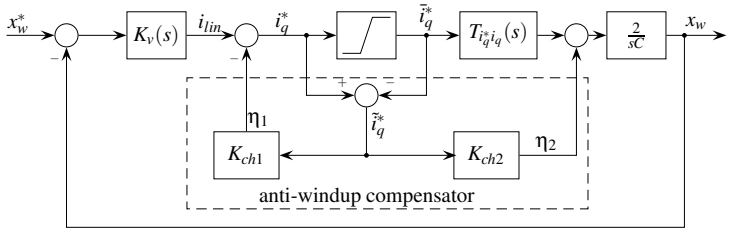

Figure 5: Simplified control scheme for AW compensator design

The inner and the outer controllers were designed with the Matlab function `hinfmix`, which implement the $\mathcal{H}_2/\mathcal{H}_\infty$ synthesis procedure with pole placement constraints [10]. Here, only the $\mathcal{H}_2$ constraints was considered but with an addition constraints on the closed loop poles location. This makes possible the controller implementation in discrete time. With this additional constraints, we are able to ensure that the controller poles are slow enough to be implemented with a sample frequency of 20 kHz.
The weights for the design of the inner controller were selected as

$$W_e = 250 \cdot I_{2\times 2}, \qquad W_u = 0.01 \cdot I_{2\times 2},$$

where $I_{2\times 2}$ denotes the identity matrix of dimension 2×2. The closed-loop poles were restricted to the sector

$$\{s \in \mathbb{C} : -2000 \leq \mathrm{Re}(s) \leq 0 \text{ and } |\mathrm{Im}(s)| \leq 2000\},$$

where $\mathbb{C}$ is the set of complex numbers and Re and Im denote the real and imaginary parts of s respectively. For the computation of the outer controller, the order of the transfer $T_{i_q^* i_q}(s)$ along with $2/sC$ was reduced in order to avoid a high order controller. The order of the controller produced by the $\mathcal{H}_2$ procedures is equal to the order of the plant plus the sum of the orders of any weighting function used to state the specifications. The weights in the outer loop case are also constants

$$W_e = 6, \qquad W_u = 0.05.$$

Finally, the anti-windup compensator K_{ch} was designed as mentioned in the previous section by solving a state feedback problem subject to $\|M(s) - I\|_\infty < 1$. This kind of problem can be solved with Matlab function `msfsyn`.
The proposed control strategy was evaluate by simulation using SimPower toolbox for Matlab in two scenarios, a change in the active power injected from the DC power source and a voltage sag in the AC electrical grid. In the first scenario the control remains all the time in normal operation whereas in the second the anti-windup compensator and the DC chopper are needed to maintain the voltage in the DC bus. The model used in the simulations includes the SVM algorithm and the switches of the IGBT. The resulting controllers discretised using the Tustin transformation for a sample frequency of 20 kHz are given in Appendix.
Figures 6 and 7 present the simulation results corresponding to the first scenario. The active power injected from the DC side is increased from 4.5 kW to 9 kW during a 100 ms period starting at 0.05 s. In Figure 6a, it can be seen the *qd* currents with the corresponding references, i_q^* is the reference produce by the outer controller to maintain the E_{DC} at 800 V. The *abc* currents are shown in Figure 6b. Finally, in Figure 6c and d, the active power and the voltage at the DC bus are shown. It can be observed that except for a very short period of time the currents do not exceed their limits indicated with dotted lines (± 20.41 A). It can be also observed the effectiveness of the outer controller to maintain the voltage in the DC bus, after the initial transients associated to the change in the power, the variable rapidly returns to the nominal value. The voltages in the *qd* are shown in Figure 7a and the voltages in the *abc* frame in Figure 7b. The control voltages produced by the SVM can be seen in Figure 7c.
The second scenario corresponds to a voltage sag of 90% deep. The so-called ride-trough capability implies that the VSC must remain connected during a voltage sag in the electrical grid. The simulation

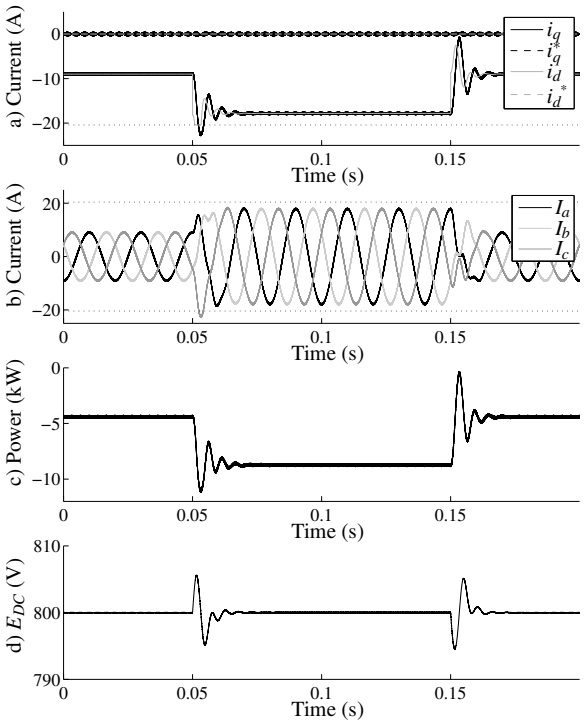

Figure 6: Simulation corresponding to the power change scenario. a) Currents in the *qd* frame, b) currents in the *abc* frame, c) active power and d) DC voltage in the DC bus

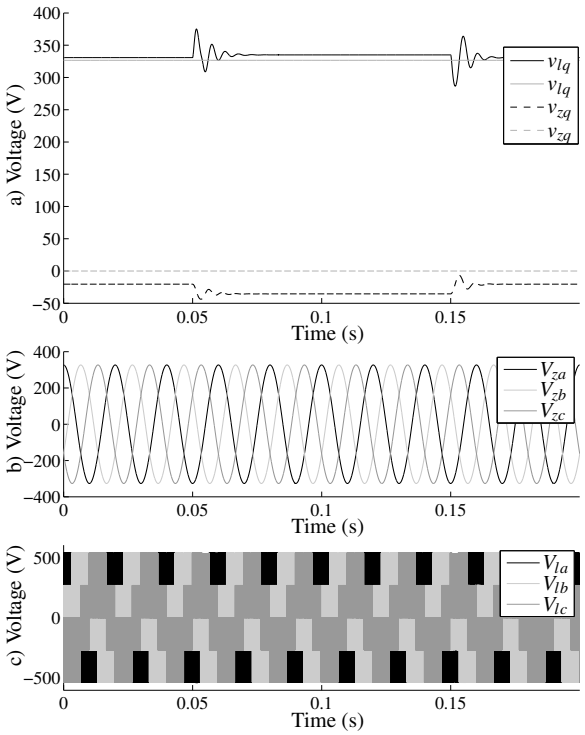

Figure 7: Simulation corresponding to the power change scenario. a) Voltages in the *qd* frame, b) grid voltages in the *abc* frame, c) converter voltages in the *abc* frame

responses are shown in Figure 8 to 10. The first figure presents the *qd* and the *abc* voltages in the grid and in the converter. In this scenario, it can be noted that the controller input does not exceed the maximum voltage levels (461.88 V) and thus no saturation effect is observed in the inner loop. Figure 8c displays the converter voltages in the *abc* frame produced by the SVM. In Figure 9a, it can be observed the currents and the corresponding references in the *qd* frame and also the currents in the *abc* frame. The maximum current limits (dotted lines) are reached during the voltage sag and as consequence the DC chopper is active during the fault. Figure 10 presents the DC voltage and the current in the chopper. In the same figure, it can be seen results obtained when a PI controller are used instead of optimal control (in the inner and in the outer loop) [6] and the DC chopper is controlled by a classical on-off strategy [11]. Notice that the AW mechanism is only active to compensate the fault. The responses shows that the proposed strategy achieves a good voltage regulation even in an extreme scenario like voltage sag of 90% deep. Compare this result with the ones corresponding to the classical control in the same scenario. Unlike the optimal option, the implementation of the on-off control of the chopper needs an offset in the DC voltage. On the other hand, the classical control exhibits a slow convergence to the nominal voltage after the disturbance. This is a consequence of the fact that the PI controller continues integrating the nonzero voltage error due to offset needed in the on-off control of the chopper.

5 Conclusions

A control scheme for VSC with a DC chopper based on multi-variable tools has been proposed. $\mathcal{H}_2$ optimal control was used in the design of the current and the voltage controllers whereas the control of the DC chopper was addressed with an AW compensation scheme.

The simulation results show a performance improvement under normal operation compared with classical controls based on decoupling and PIs. Nevertheless, the most noticeable improvement can be observed under severe voltage sags where the chopper is needed to maintain the DC voltage. In this situation, the proposed optimal AW controller provides a more effective control of the chopper achieving a faster

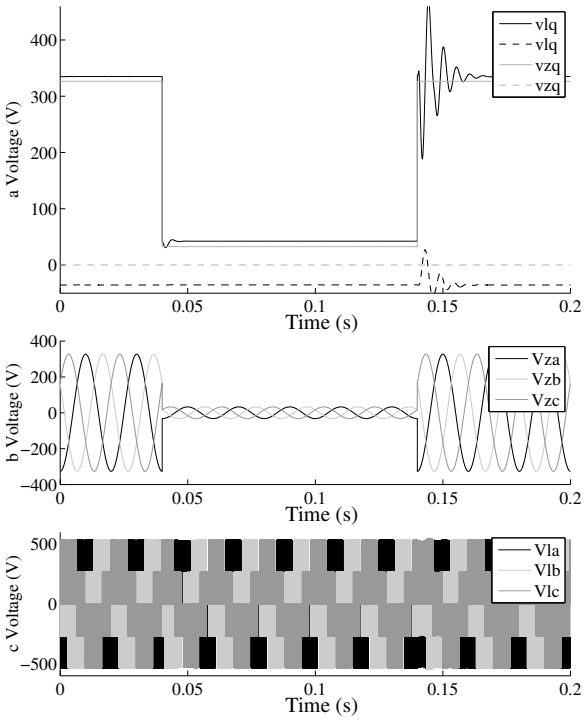

Figure 8: Simulation corresponding to the voltage sag scenario. a) Voltages in the *qd* frame, b) grid voltages in the *abc* frame, c) converter voltages in the *abc* frame

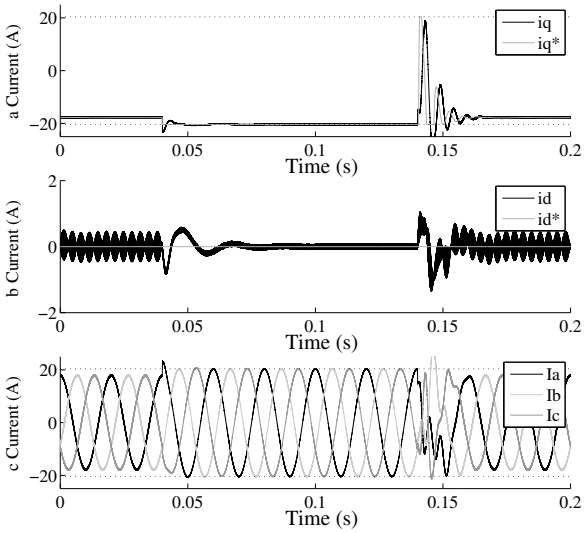

Figure 9: Simulation corresponding to the voltage sag scenario. a) q component of the currents, b) d component of the currents and c) currents in the *abc* frame

convergence of the DC voltage to its nominal value.
The orders of the proposed controllers are higher than classical PI schemes and thus the implementation may result more complex. However, this small disadvantage is compensated by the improvement in the ride-through capability of the VSC. On the other hand, the proposed scheme can be easily extended to deal with more complex phenomena such as model uncertainty and unbalance input voltages.

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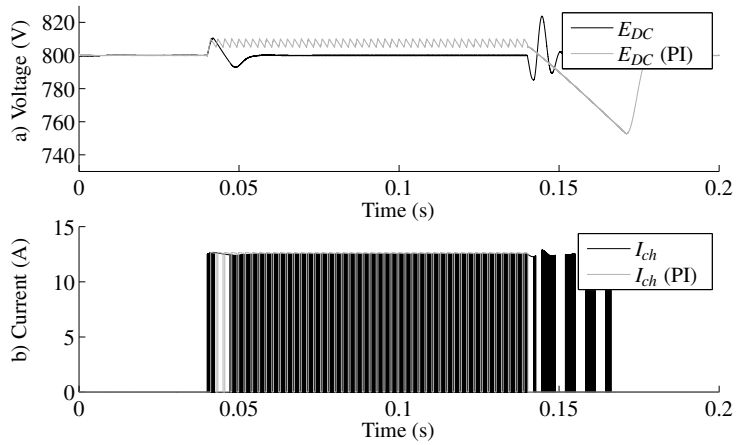

Figure 10: Simulation corresponding to the voltage sag scenario, comparison between the proposed control (black lines) and classical control strategy (grey lines). a) DC voltages, b) currents in the chopper

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Appendix

Discrete controllers (sample frequency 20 kHz) used in simulations

$$K_c(z) = \left[\begin{array}{cccccc|cc} 1.00 & 0.00 & 0.00 & 0.00 & 0.00 & 0.00 & 2.06 & -0.00 \\ 0.00 & 1.00 & 0.00 & 0.00 & 0.00 & 0.00 & -0.00 & -2.06 \\ 0.00 & 0.00 & 0.96 & -0.01 & -0.08 & 0.00 & 0.40 & 0.26 \\ 0.00 & 0.00 & 0.01 & 0.96 & -0.00 & -0.08 & 0.26 & -0.40 \\ 0.00 & 0.00 & 0.08 & -0.02 & 0.84 & 0.02 & -0.27 & -0.31 \\ 0.00 & 0.00 & 0.02 & 0.08 & -0.02 & 0.84 & -0.31 & 0.27 \\ \hline -0.01 & 0.04 & -0.26 & -0.40 & -0.25 & -0.33 & -0.02 & -0.00 \\ 0.04 & 0.01 & -0.40 & 0.26 & -0.33 & 0.25 & 0.00 & -0.02 \end{array}\right],$$

$$K_v(z) = \left[\begin{array}{ccccc|c} 1.00 & 0.00 & 0.00 & 0.00 & 0.00 & 0.35 \\ 0.00 & 0.96 & 0.09 & 0.01 & 0.04 & 0.13 \\ 0.00 & -0.09 & 0.98 & -0.01 & -0.04 & 0.07 \\ 0.00 & 0.01 & 0.01 & 0.99 & -0.10 & -0.01 \\ 0.00 & -0.04 & -0.04 & 0.10 & 0.79 & 0.08 \\ \hline 0.01 & 0.13 & -0.07 & -0.01 & -0.08 & 0.00 \end{array}\right],$$

$$K_{ch}(z) = \left[\begin{array}{ccc|c} 0.94 & -0.01 & -0.04 & 0.22 \\ -0.12 & 0.89 & -0.00 & 0.23 \\ -0.04 & -0.10 & 0.87 & 0.09 \\ \hline -0.19 & -0.21 & -0.07 & -0.05 \\ 0.09 & -0.12 & 0.08 & 0.00 \end{array}\right],$$

where

$$K(z) = C(zI - A)^{-1}B + D = \left[\begin{array}{c|c} A & B \\ \hline C & D \end{array}\right].$$